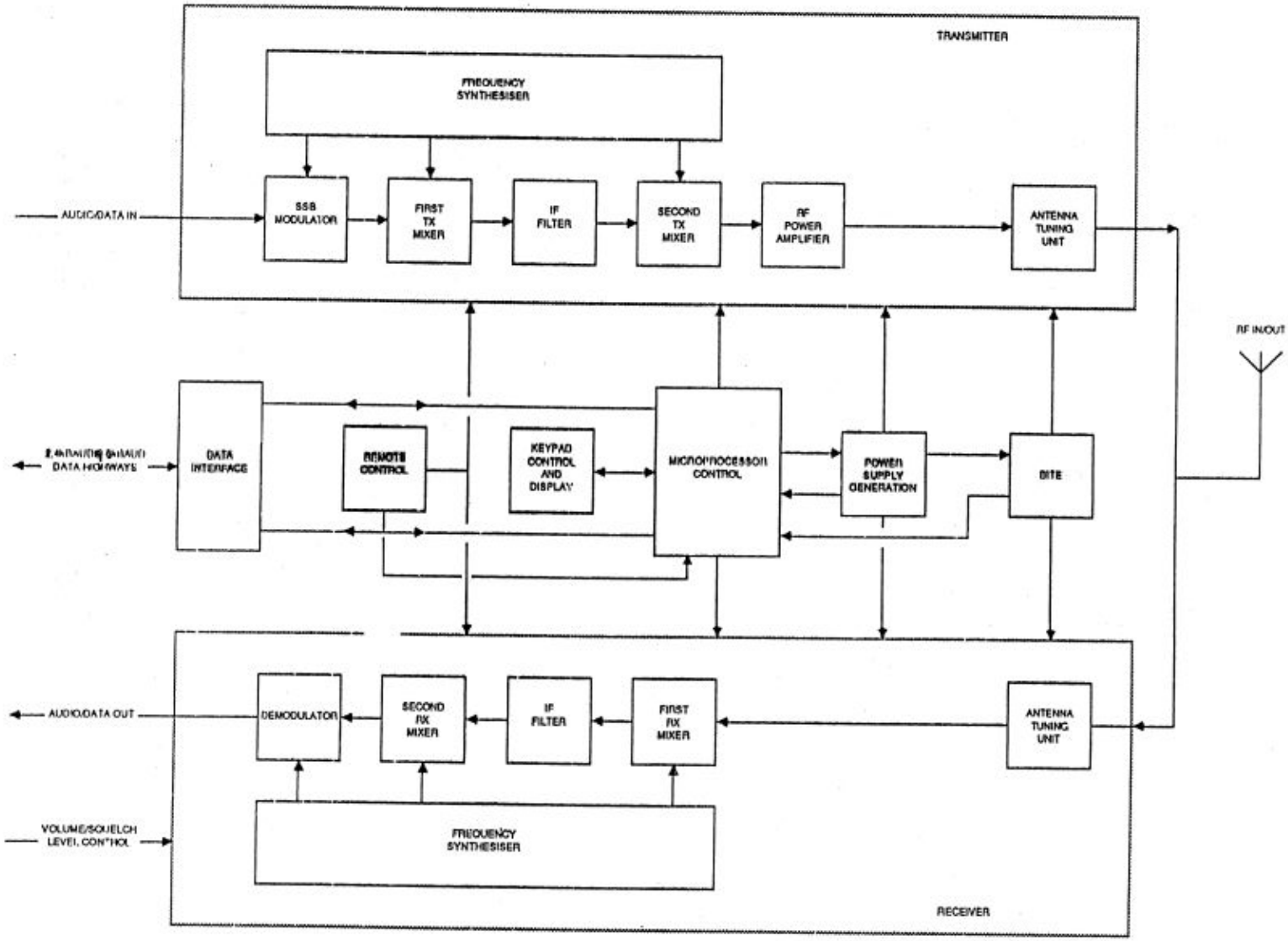

TRANSMITTER
FREQUENCY SYNTHESISER
AUDIO/DATA IN
SSB MODULATOR
FIRST TX MIXER
IF FILTER
SECOND TX MIXER
RF POWER AMPLIFIER
ANTENNA TUNING UNIT
RF IN/OUT
DATA INTERFACE
REMOTE CONTROL
KEYPAD CONTROL AND DISPLAY
MICROPROCESSOR CONTROL
POWER SUPPLY GENERATION
BITE
AUDIO/DATA OUT
DEMODULATOR
SECOND RX MIXER
IF FILTER
FIRST RX MIXER
ANTENNA TUNING UNIT
VOLUME/SQUELCH LEVEL CONTROL
FREQUENCY SYNTHESISER
RECEIVER

FIGURE 1

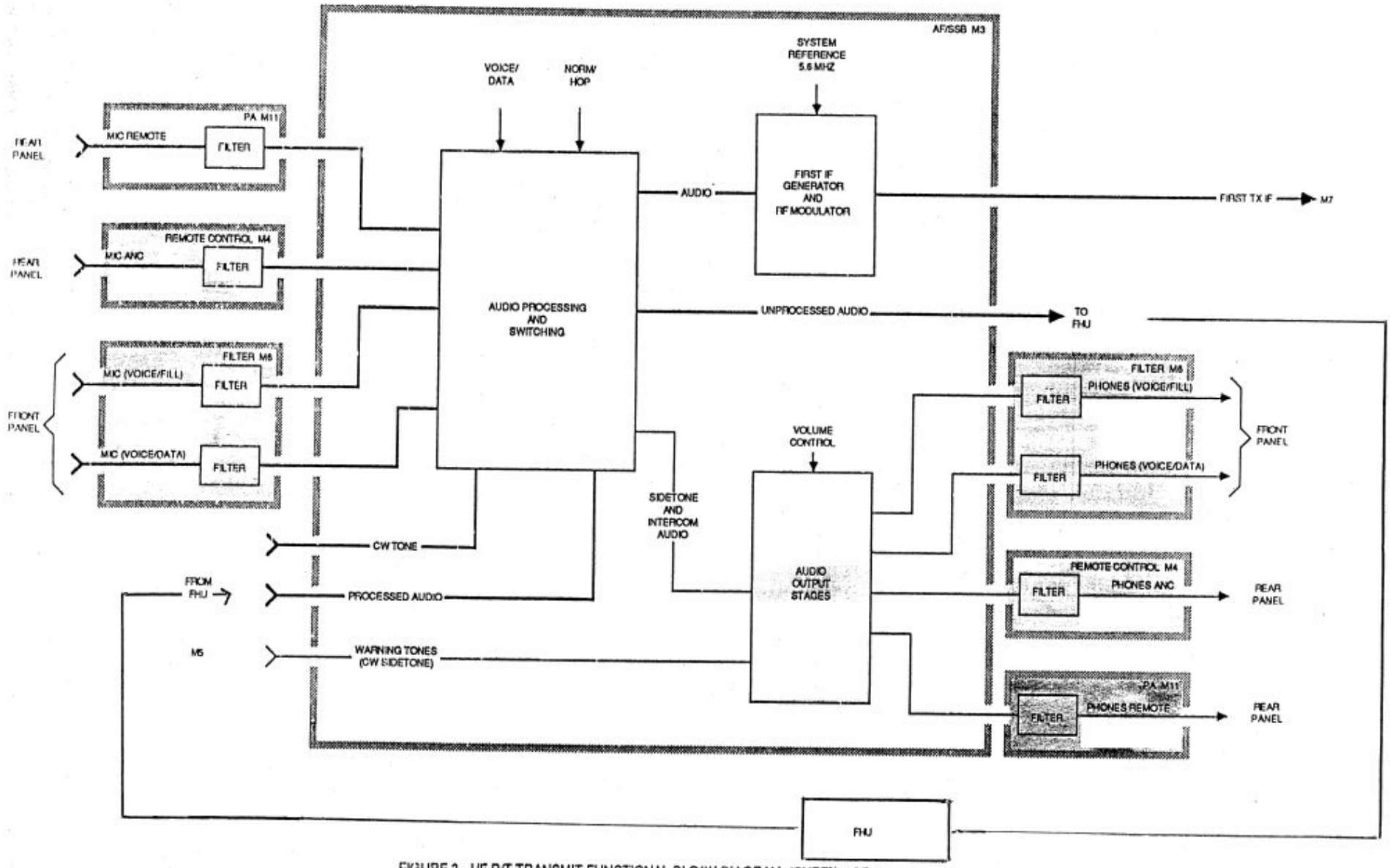


FIGURE 3 - HF R/T TRANSMIT FUNCTIONAL BLOCK DIAGRAM (SHEET 1 OF 3)

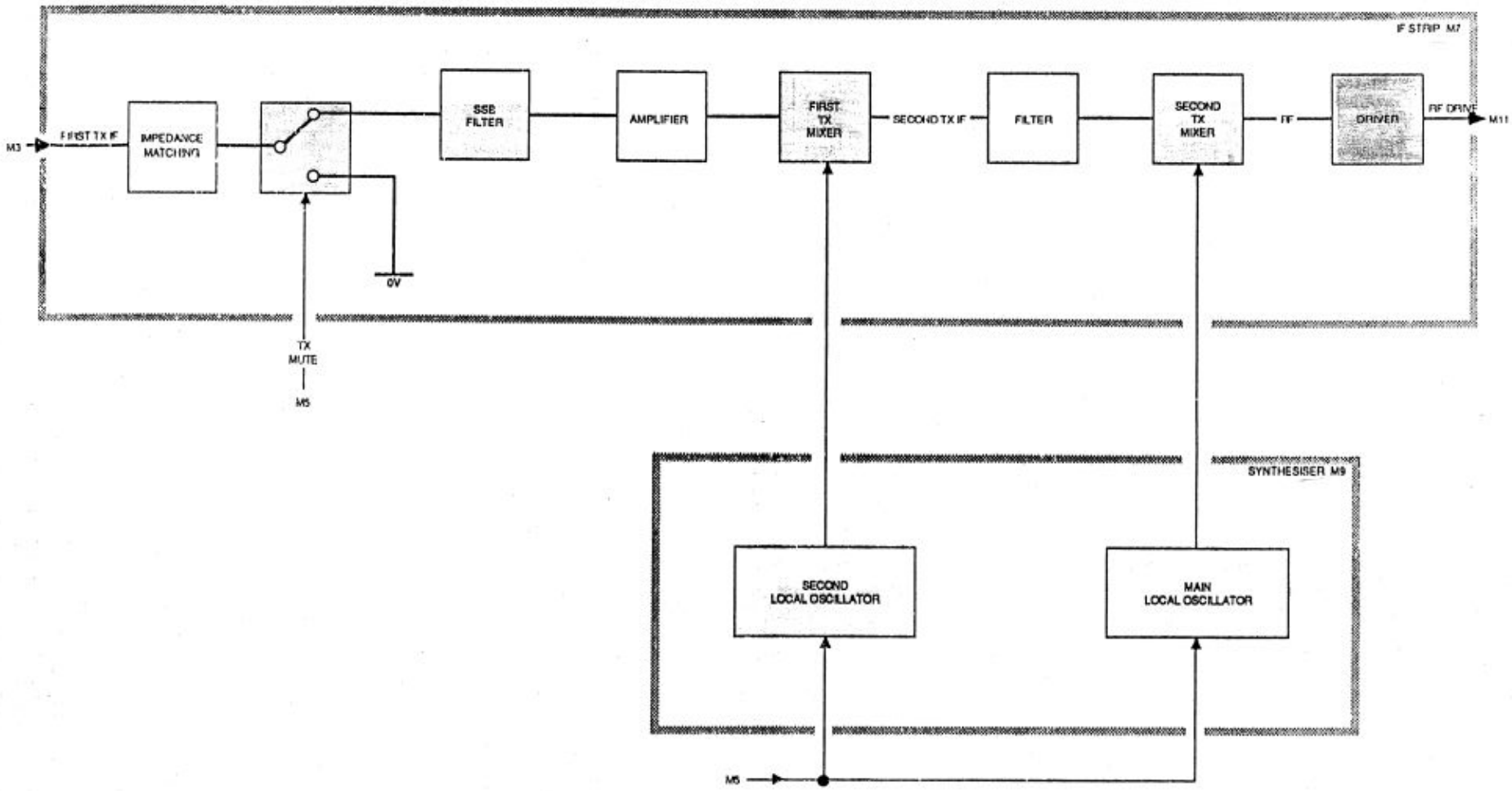


FIGURE 3 - HF R/T TRANSMIT FUNCTIONAL BLOCK DIAGRAM (SHEET 2 OF 3)

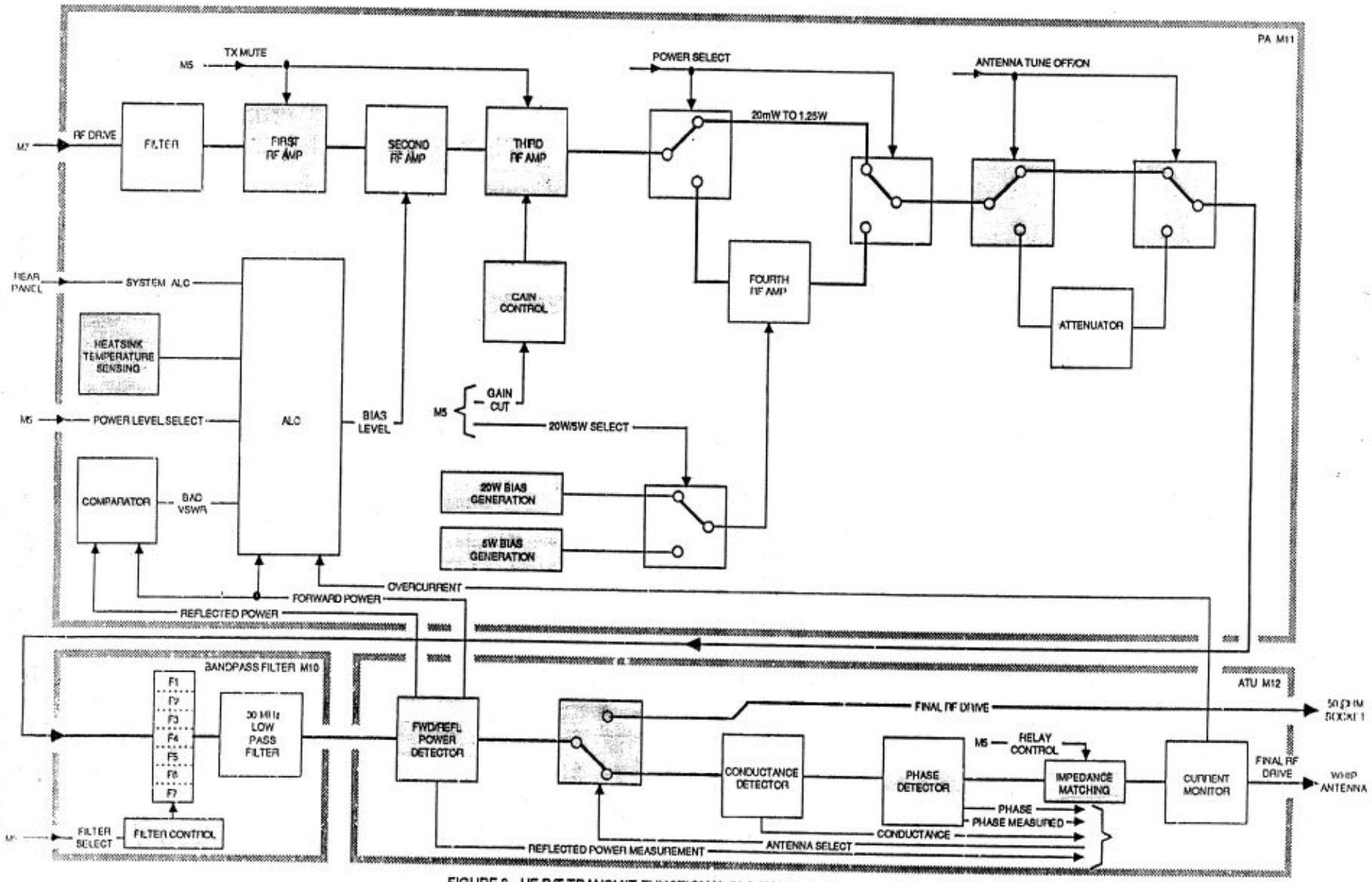


FIGURE 3 - HF R/T TRANSMIT FUNCTIONAL BLOCK DIAGRAM (SHEET 3 OF 3)

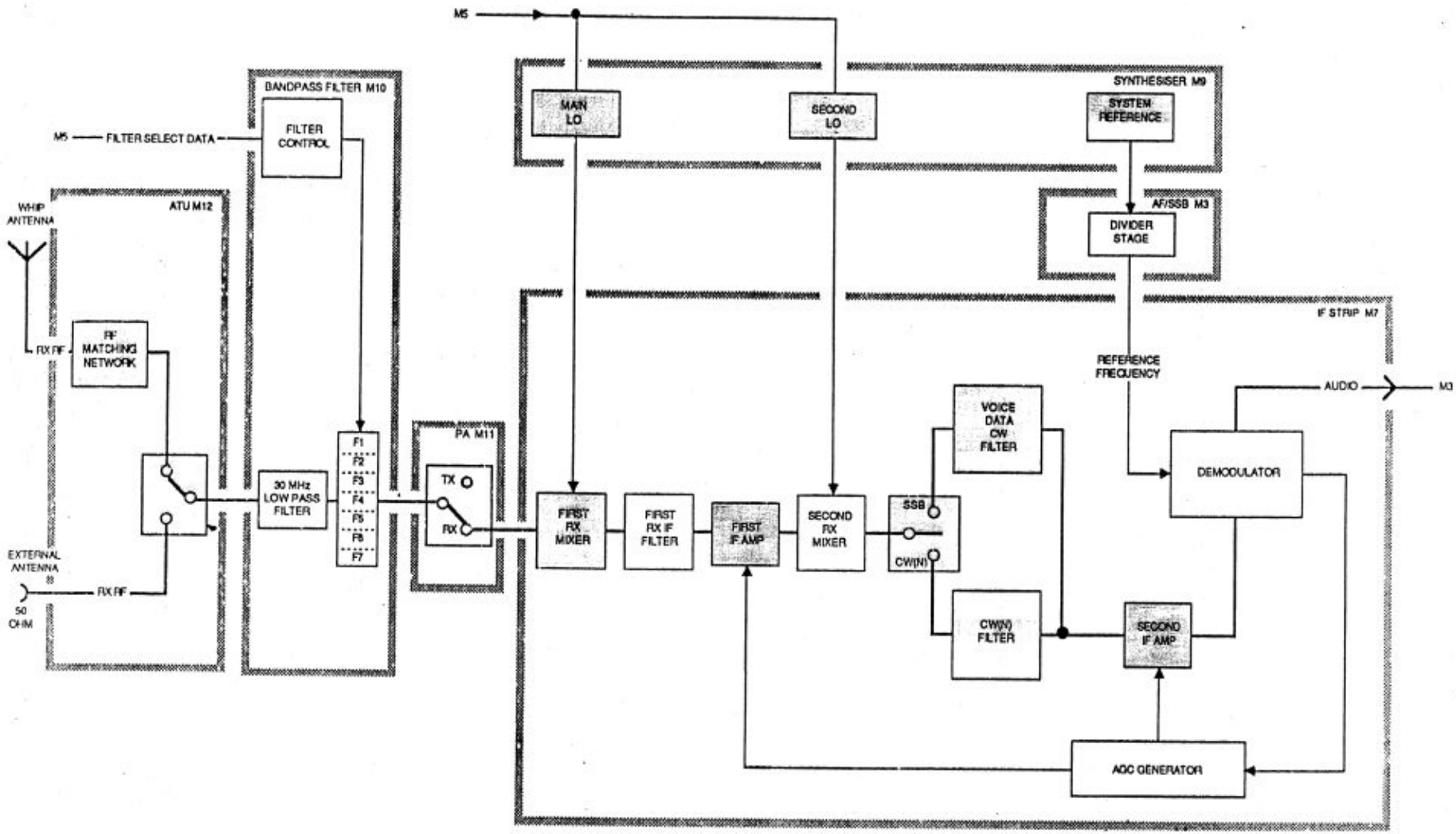


FIGURE 4 - HF R/T RECEIVER FUNCTIONAL BLOCK DIAGRAM (SHEET 1 of 2)

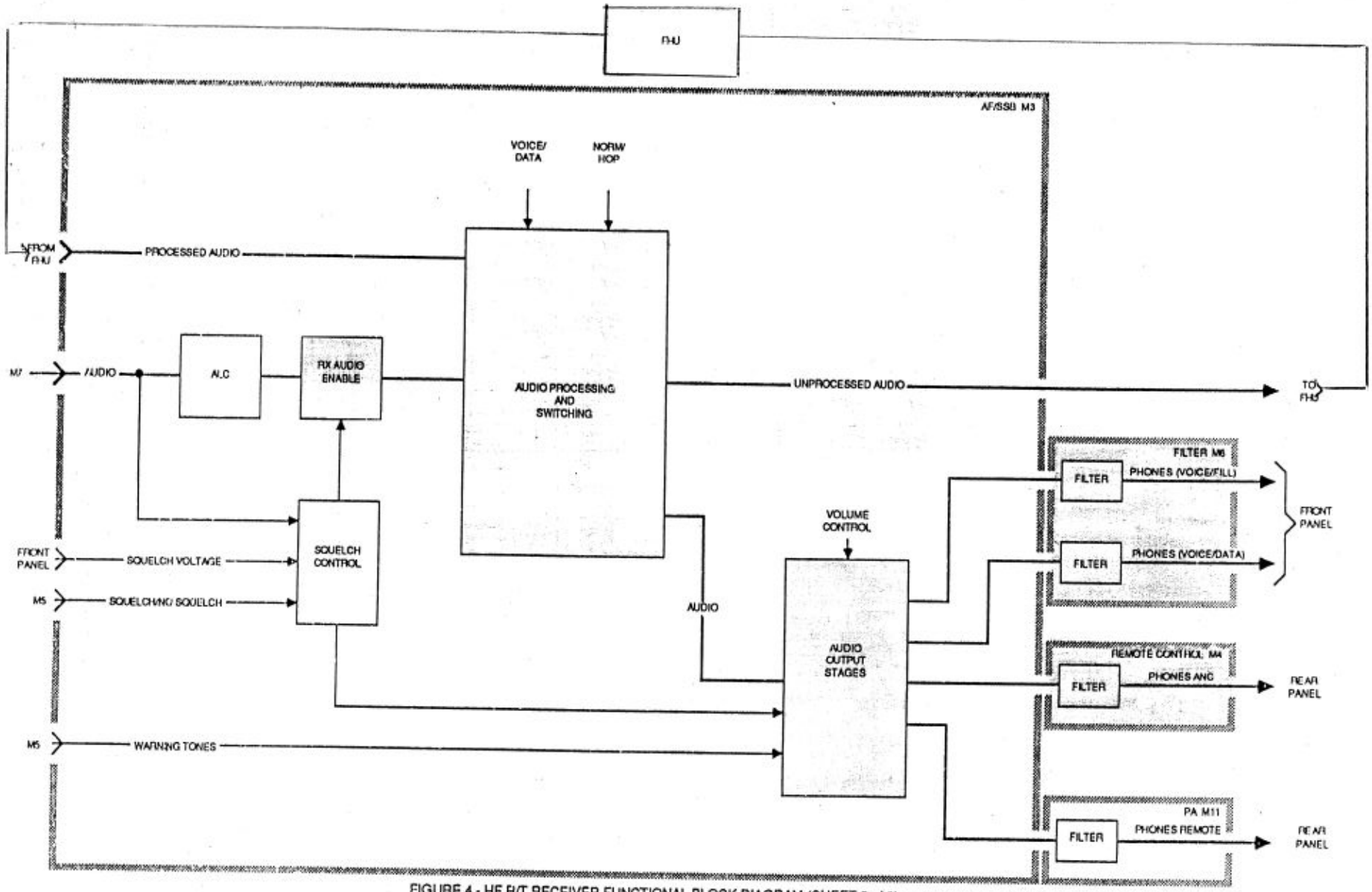
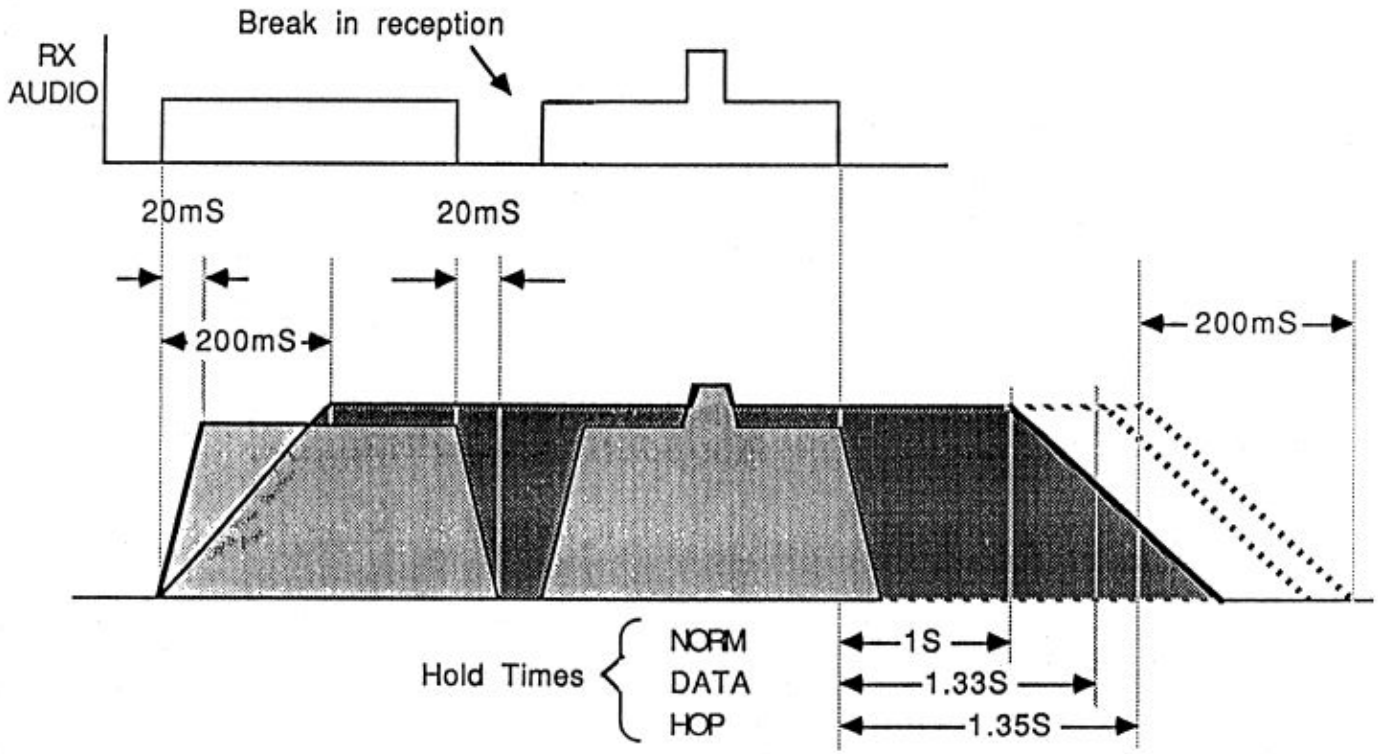


FIGURE 4 - HF R/T RECEIVER FUNCTIONAL BLOCK DIAGRAM (SHEET 2 of 2)

RT - F100 EQUIPMENT FUNCTIONAL DIAGRAM LAYOUT

Module 7	Module 11	Module 10
Module 6	Module 4	Module 12

AGC OPERATION

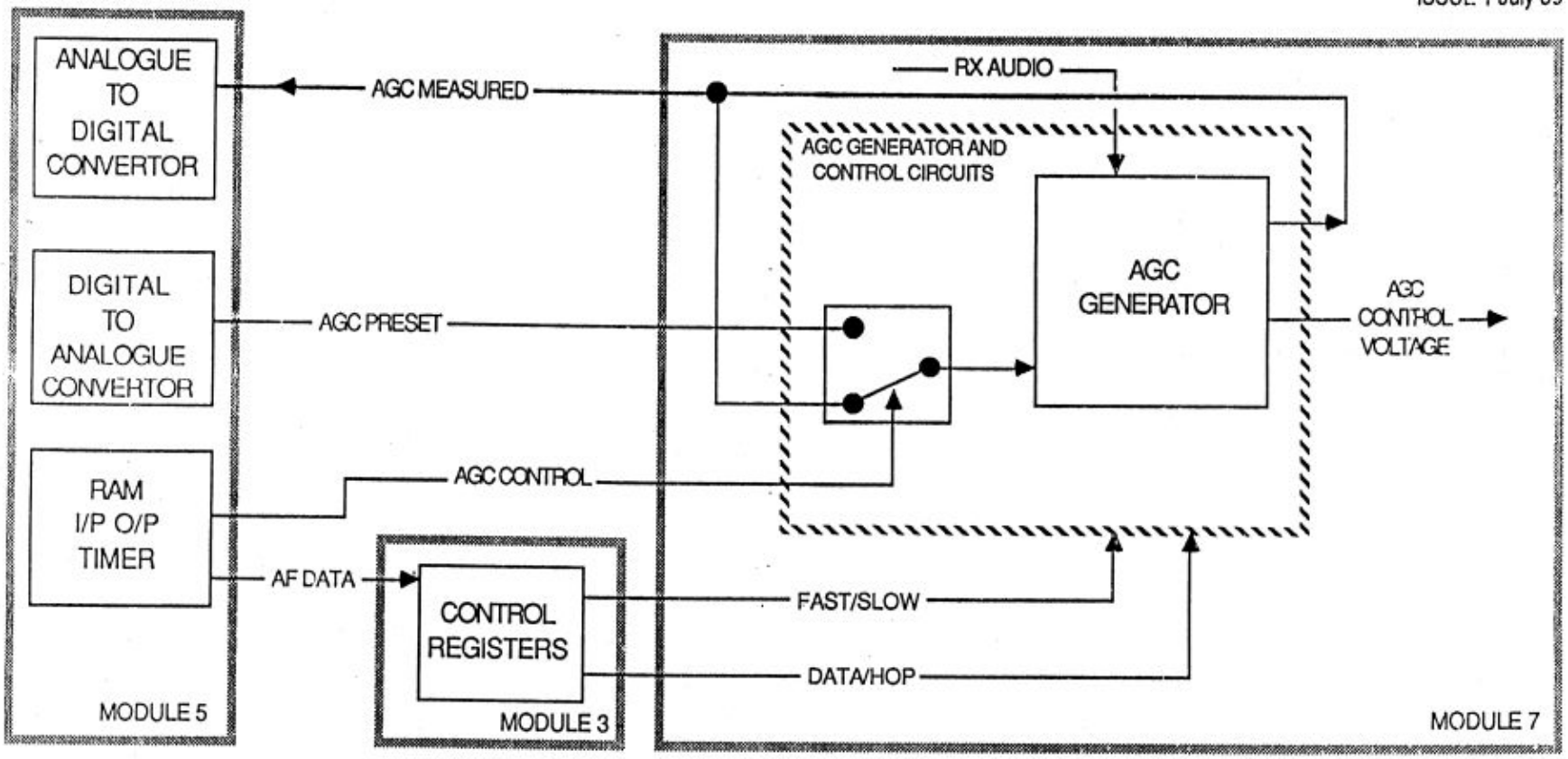


AGC Control Voltage Level

Short Time Constant Detector Ouput

Long Time Constant Detector Output

FIGURE 11



	FAST/SLOW	DATA/HOP	HOLD TIME
SSB/CW	1	0	1 SEC
DATA	0	1	1.33 SEC
HOP	0	0	1.35 SEC

FIGURE 12

RESULT OF NORMAL AGC APPLIED TO HOPPING SIGNAL

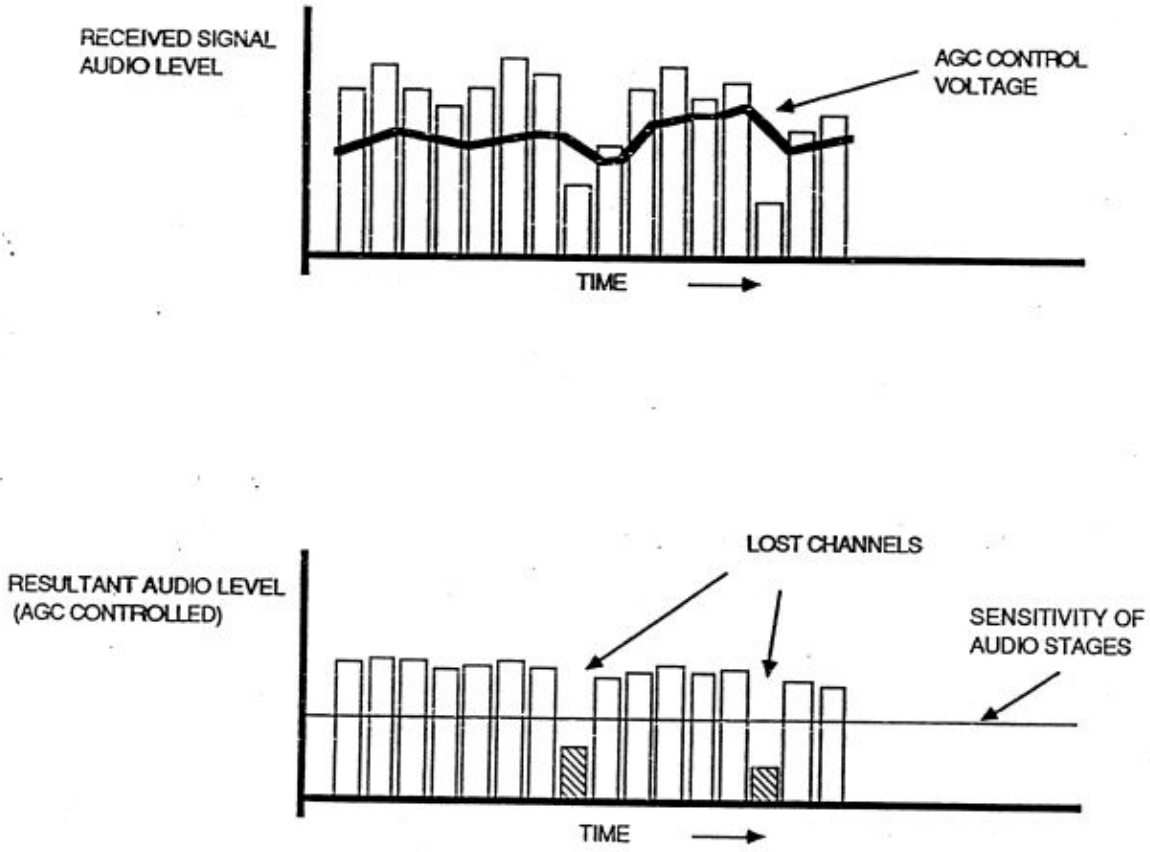
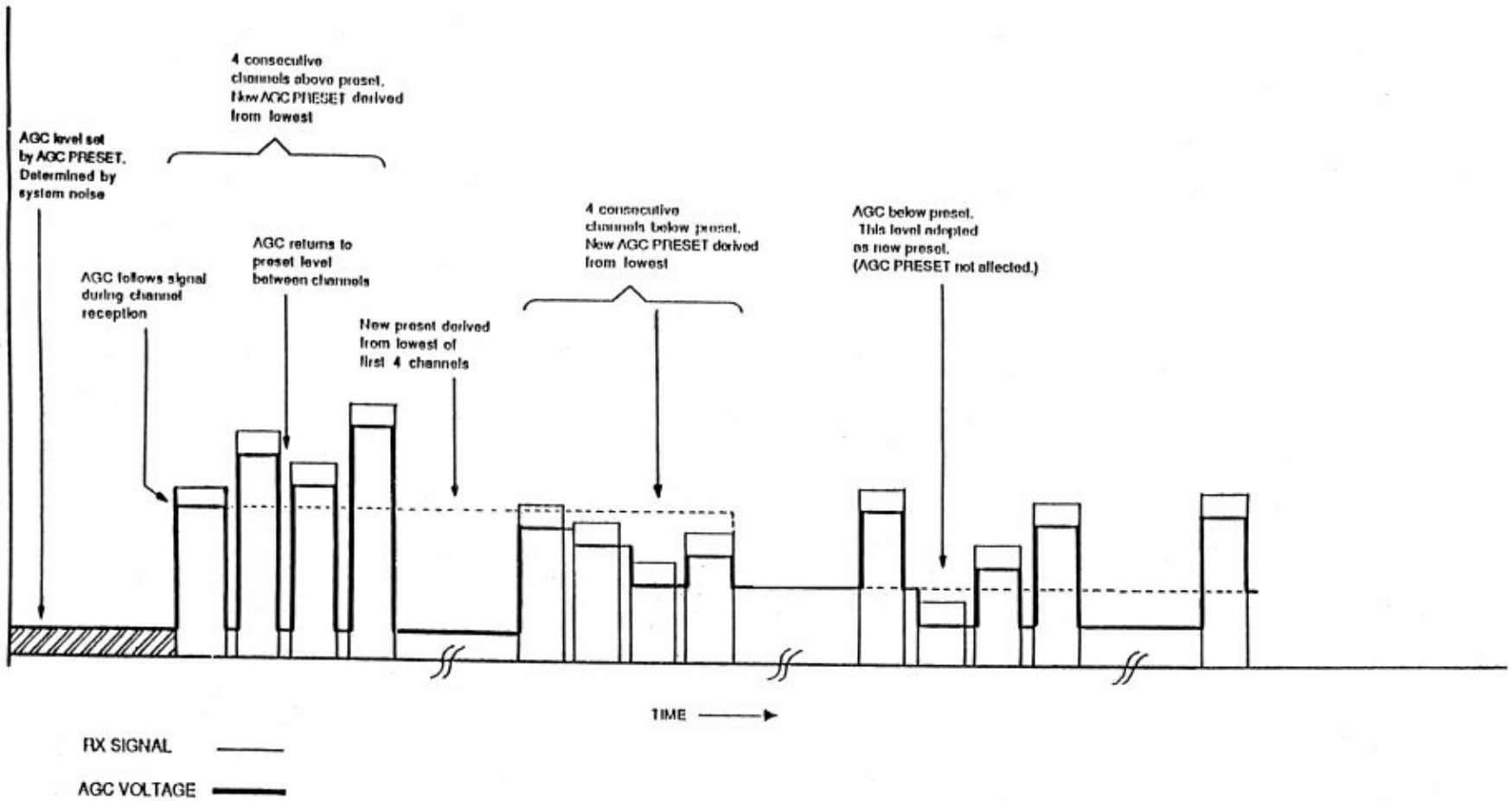


FIGURE 13

MICROPROCESSOR CONTROLLED AGC.



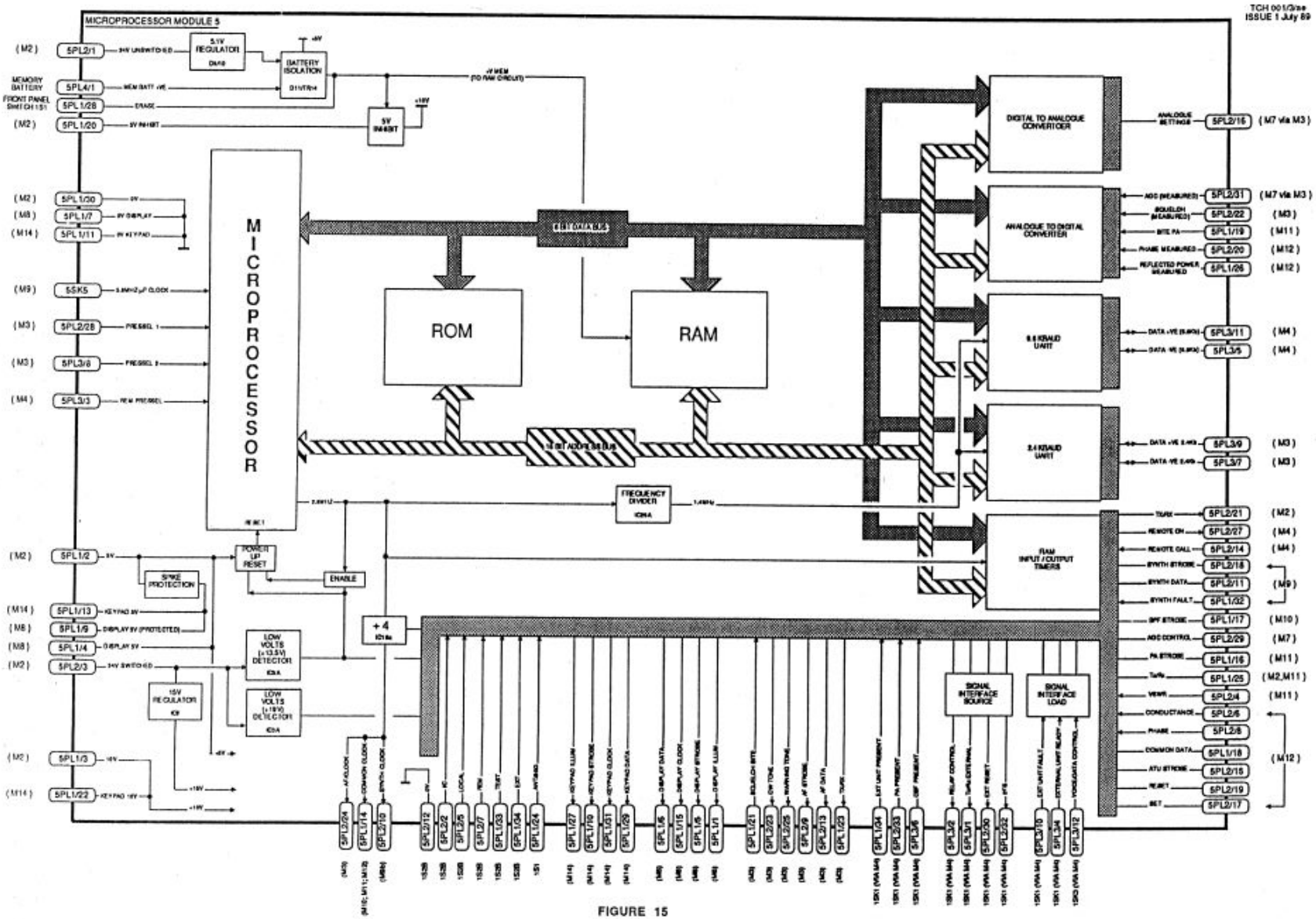

MICROPROCESSOR MODULE 5
TCH 001/Issue
ISSUE 1 July 89
MICROPROCESSOR
ROM
RAM
DIGITAL TO ANALOGUE CONVERTER
ANALOGUE TO DIGITAL CONVERTER
FREQUENCY DIVIDER
POWER UP RESET
SPIKE PROTECTION
ENABLE
LOW VOLTS DETECTOR
15V REGULATOR
BATTERY ISOLATION
5V REGULATOR
5V INHIBIT
SIGNAL INTERFACE SOURCE
SIGNAL INTERFACE LOAD
MEMORY BATTERY
FRONT PANEL SWITCH
(M2)
(M8)
(M14)
(M9)
(M3)
(M4)
(M7 via M3)
(M11)
(M12)
(M10)
(M7)
(M2,M11)
(M12)

FIGURE 15

FRONT PANEL DISPLAY AND CONTROLS

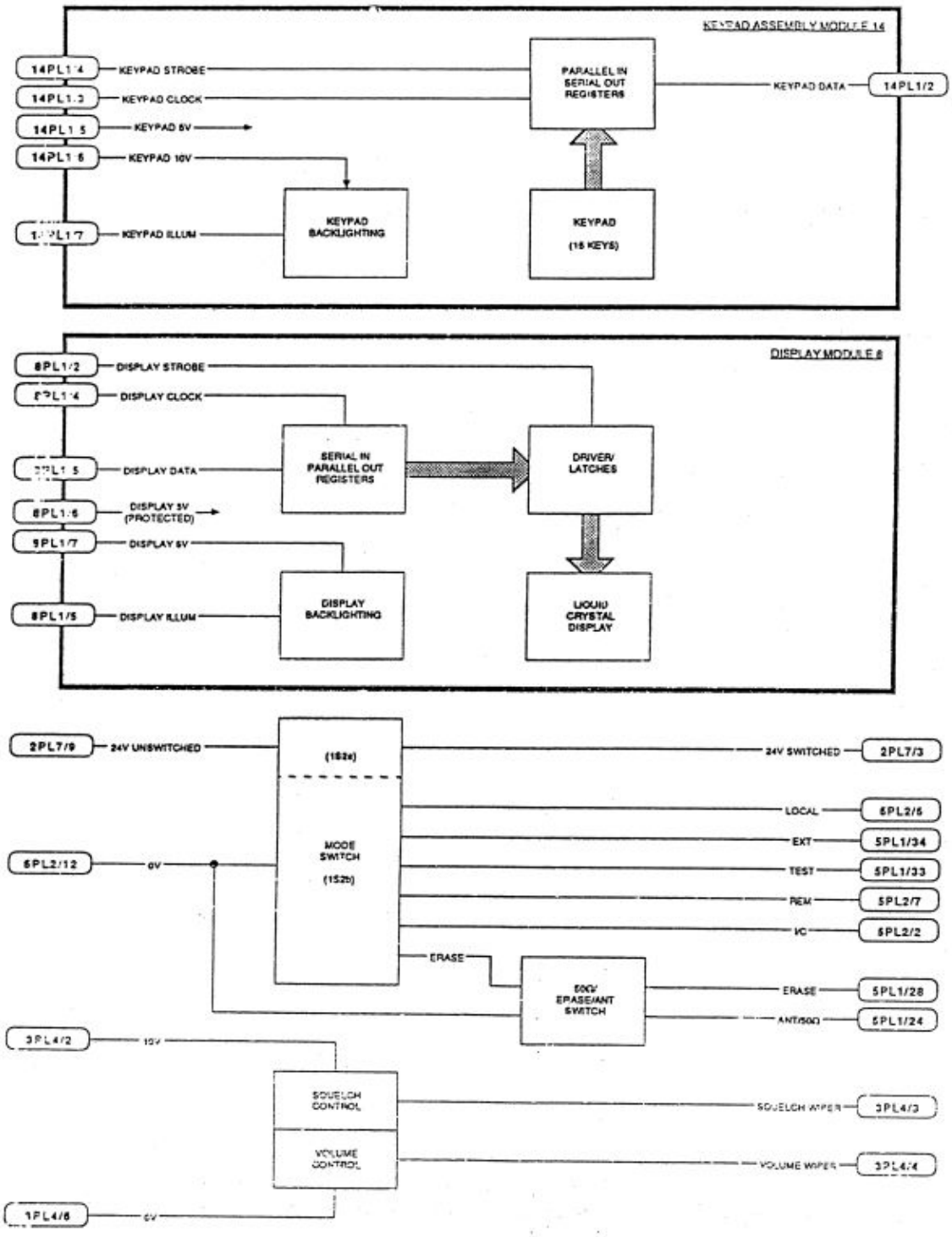


FIGURE 16

SYNTHESISER MODULE 9

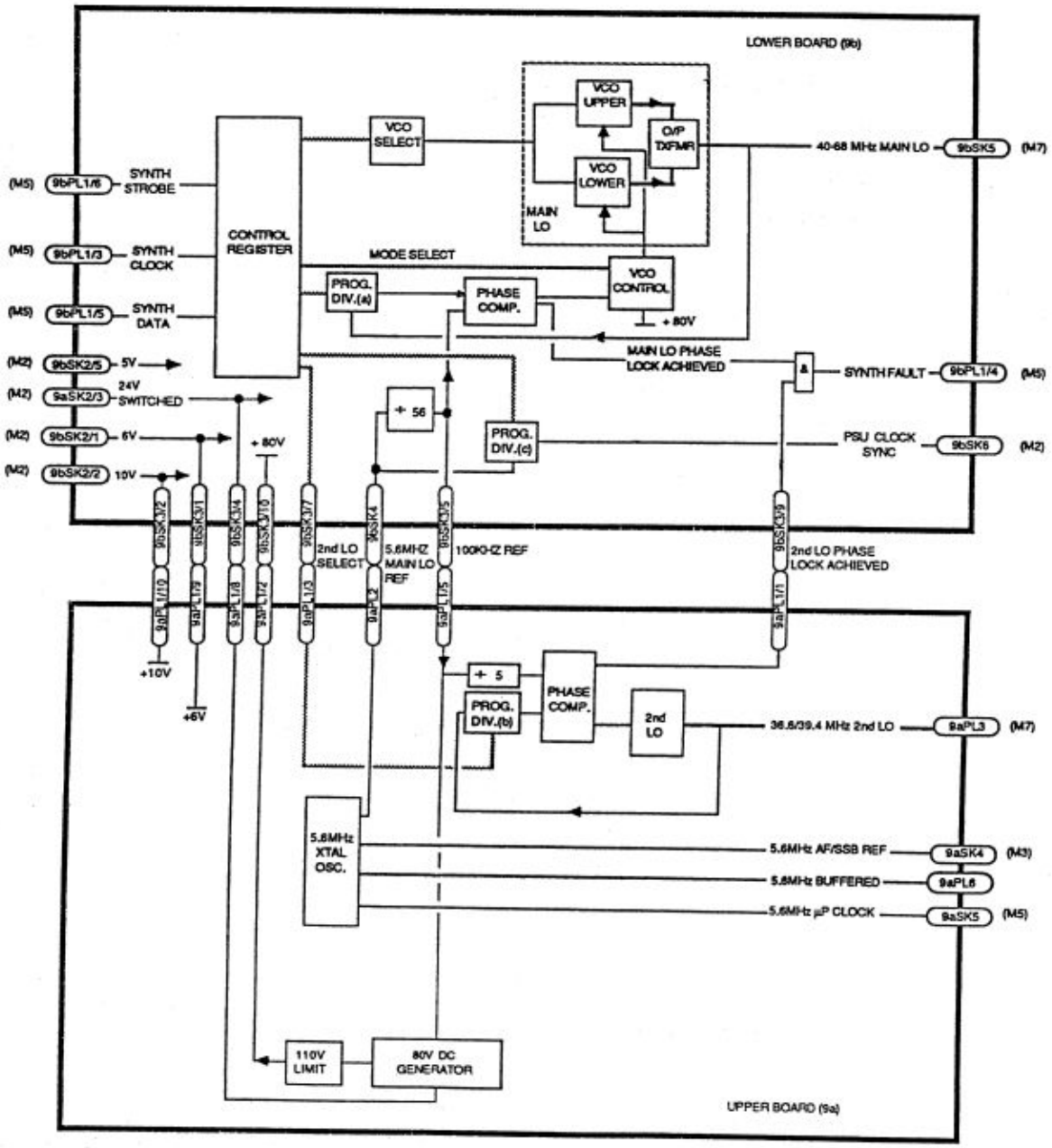


FIGURE 17

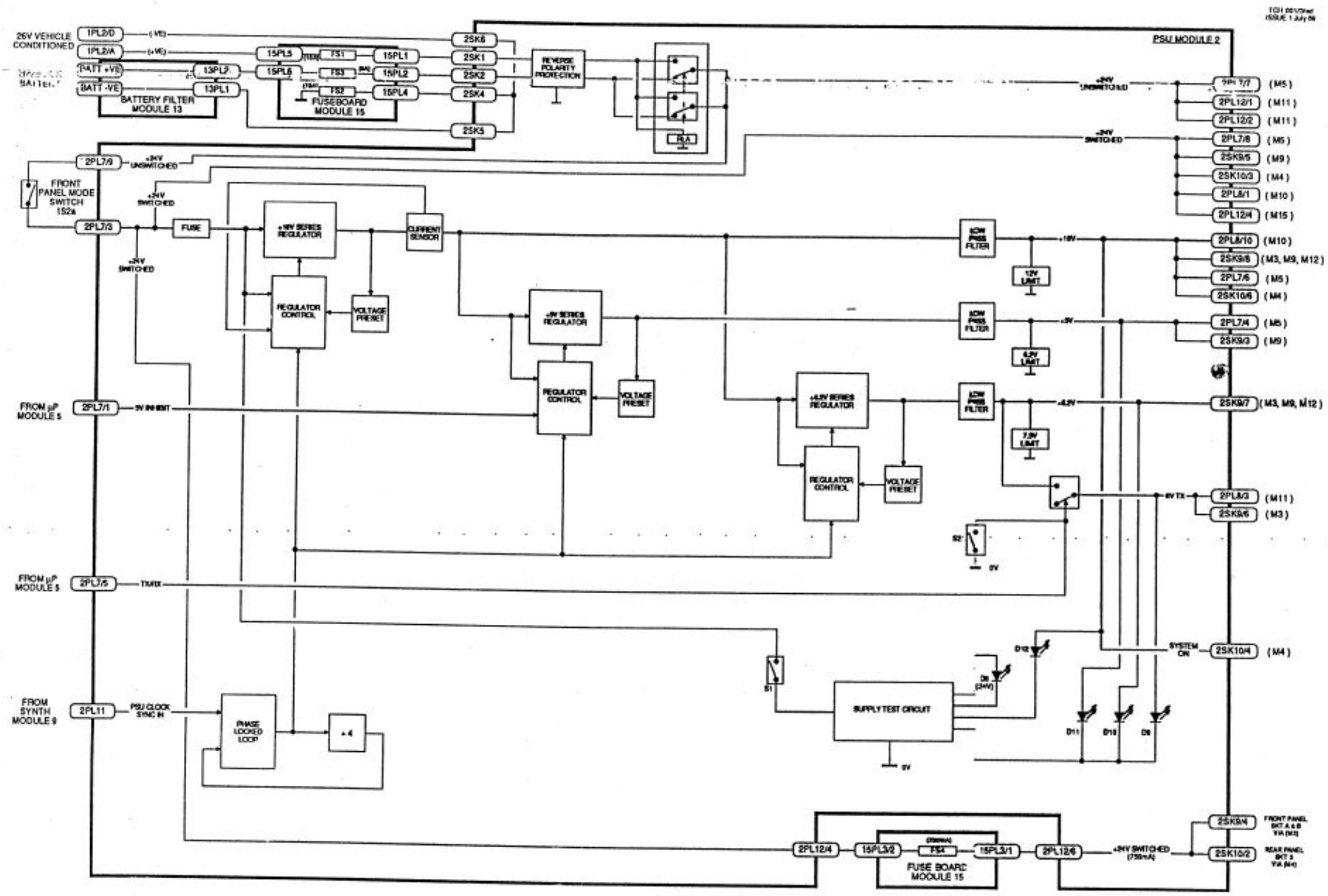

26V VEHICLE CONDITIONED
1PL2/D
1PL2/A
(BATT +VE)
(BATT -VE)
13PL2
13PL1
BATTERY FILTER MODULE 13
15PL5
15PL6
FS1
FS3
FS2
15PL1
15PL2
15PL4
FUSEBOARD MODULE 15
2SK6
2SK1
2SK2
2SK4
2SK5
REVERSE POLARITY PROTECTION
PSU MODULE 2
2PL7/9
+24V UNSWITCHED
FRONT PANEL MODE SWITCH 152a
2PL7/3
+24V SWITCHED
FUSE
+18V SERIES REGULATOR
CURRENT SENSOR
REGULATOR CONTROL
VOLTAGE PRESET
+9V SERIES REGULATOR
+6.2V SERIES REGULATOR
LOW PASS FILTER
12V LIMIT
6.2V LIMIT
7.5V LIMIT
FROM µP MODULE 5
2PL7/1
5V INHIBIT
2PL7/5
TX/RX
FROM SYNTH MODULE 9
2PL11
PSU CLOCK SYNC IN
PHASE LOCKED LOOP
÷4
SUPPLY TEST CIRCUIT
SYSTEM ON
FUSE BOARD MODULE 15
2PL12/4
15PL3/2
15PL3/1
2PL12/6
2PL7/7
2PL12/1
2PL12/2
2PL7/8
2SK9/5
2SK10/3
2PL8/1
2PL12/4
2PL8/10
2SK9/8
2PL7/6
2SK10/6
2PL7/4
2SK9/3
2SK9/7
2PL8/3
2SK9/6
2SK10/4
2SK9/4
2SK10/2
(M5)
(M11)
(M11)
(M5)
(M9)
(M4)
(M10)
(M15)
(M10)
(M3, M9, M12)
(M5)
(M4)
(M5)
(M9)
(M3, M9, M12)
(M11)
(M3)
(M4)

FIGURE 18

BITE FUNCTIONAL DIAGRAM

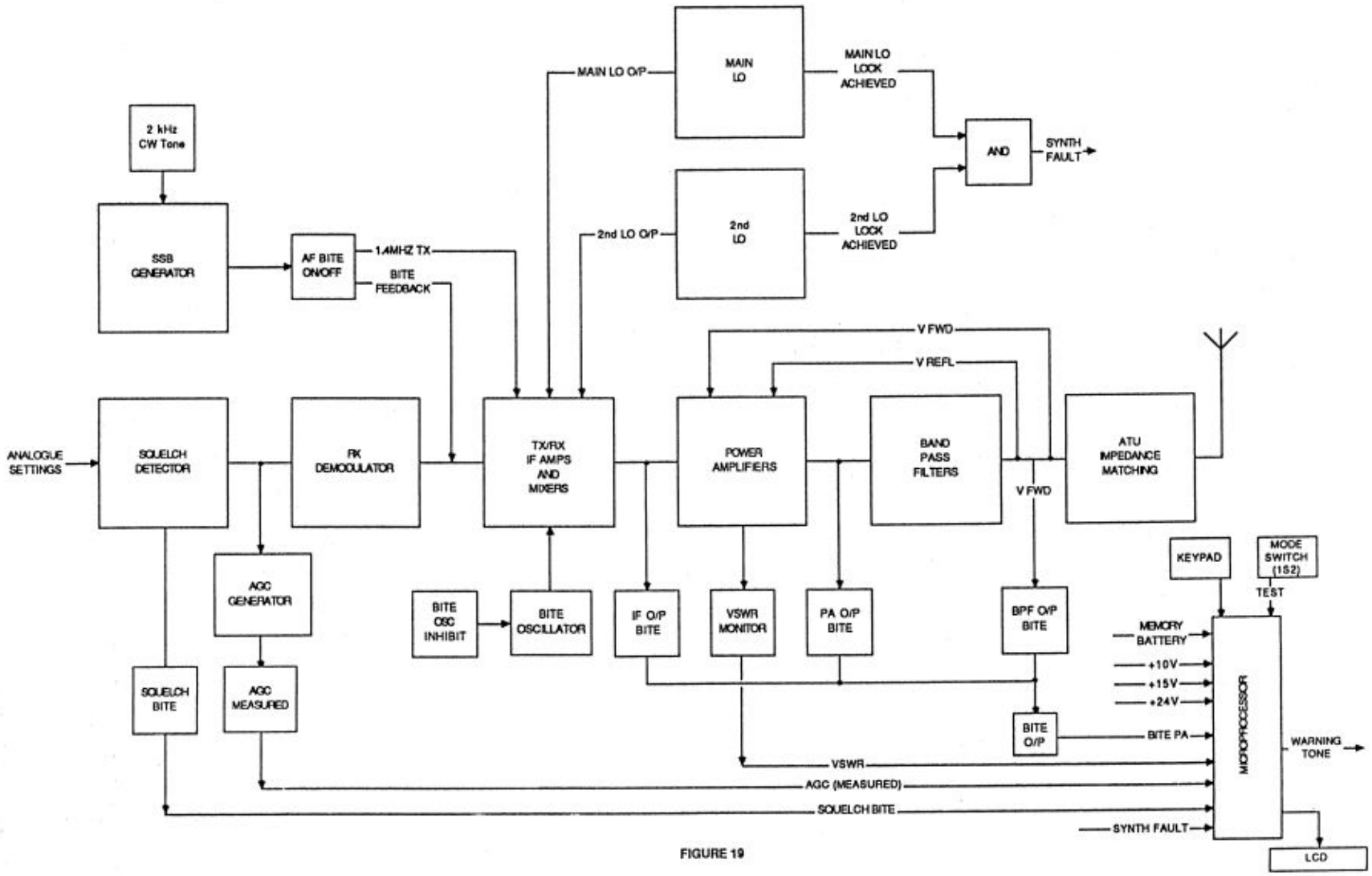


FIGURE 19

POSSIBLE SYSTEM CONFIGURATIONS

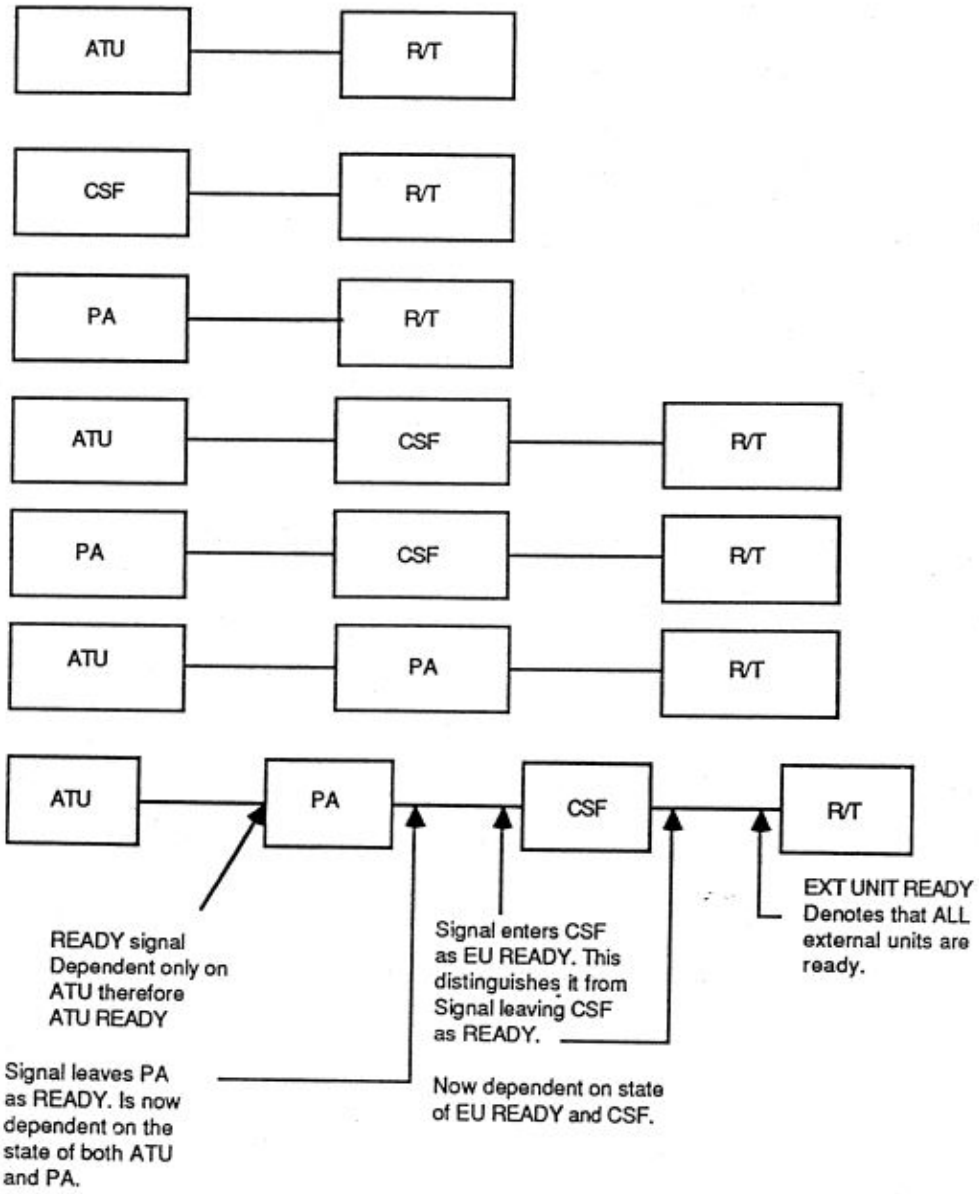


FIGURE 20.

VOICE SIDETONE

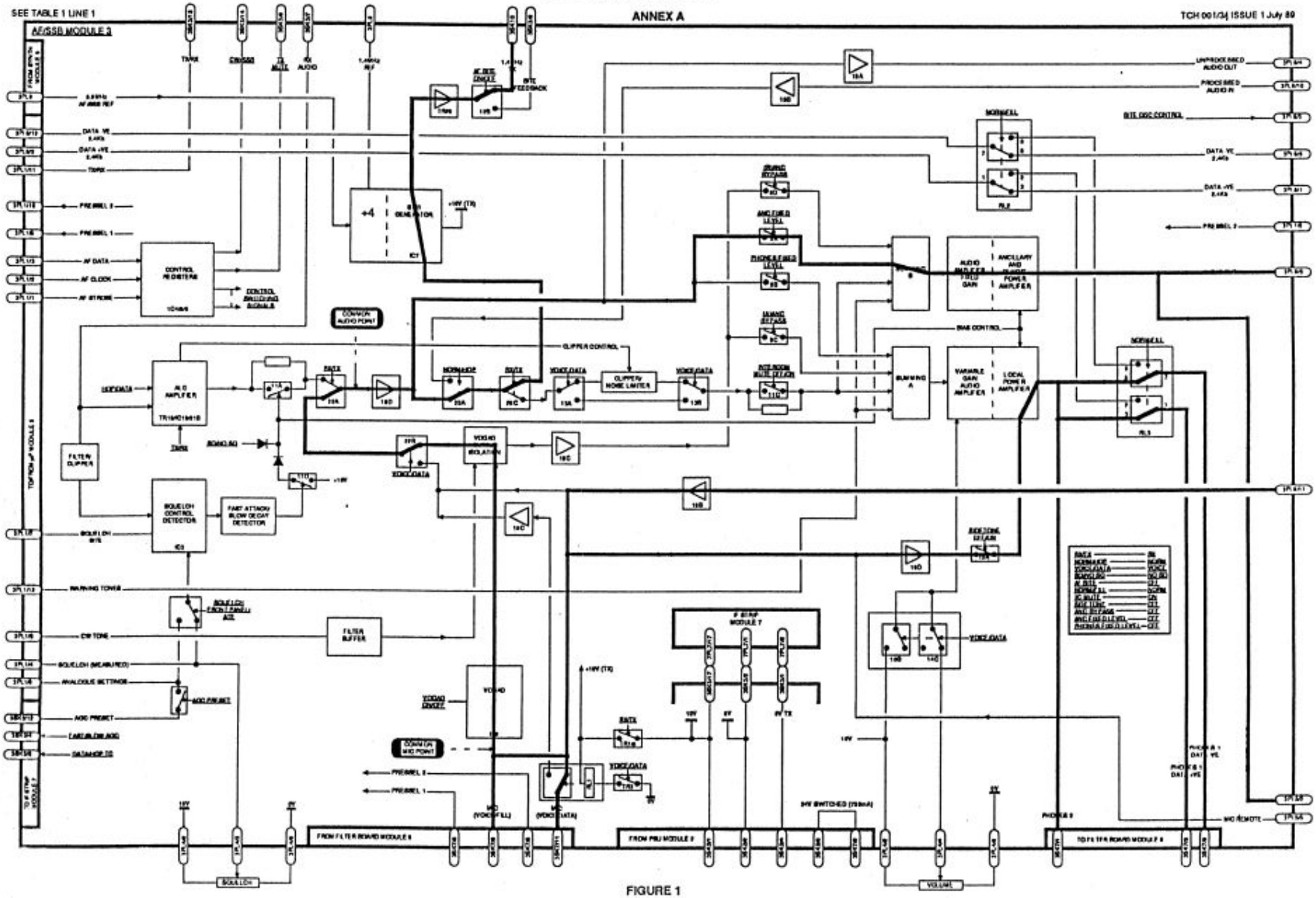


FIGURE 1

DATA SIDETONE

ANNEX A

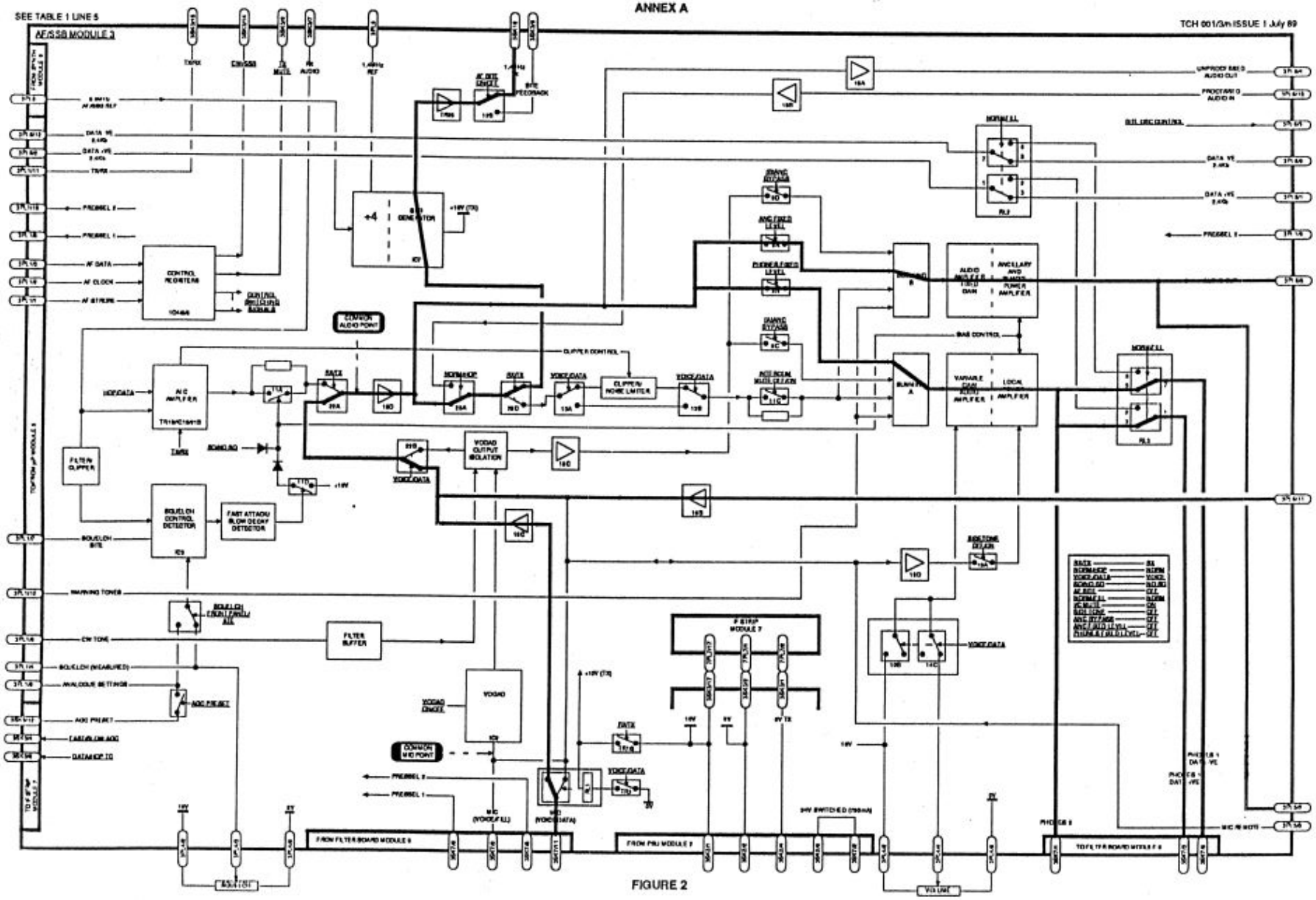


FIGURE 2

ANCILLARY & REMOTE AUDIO

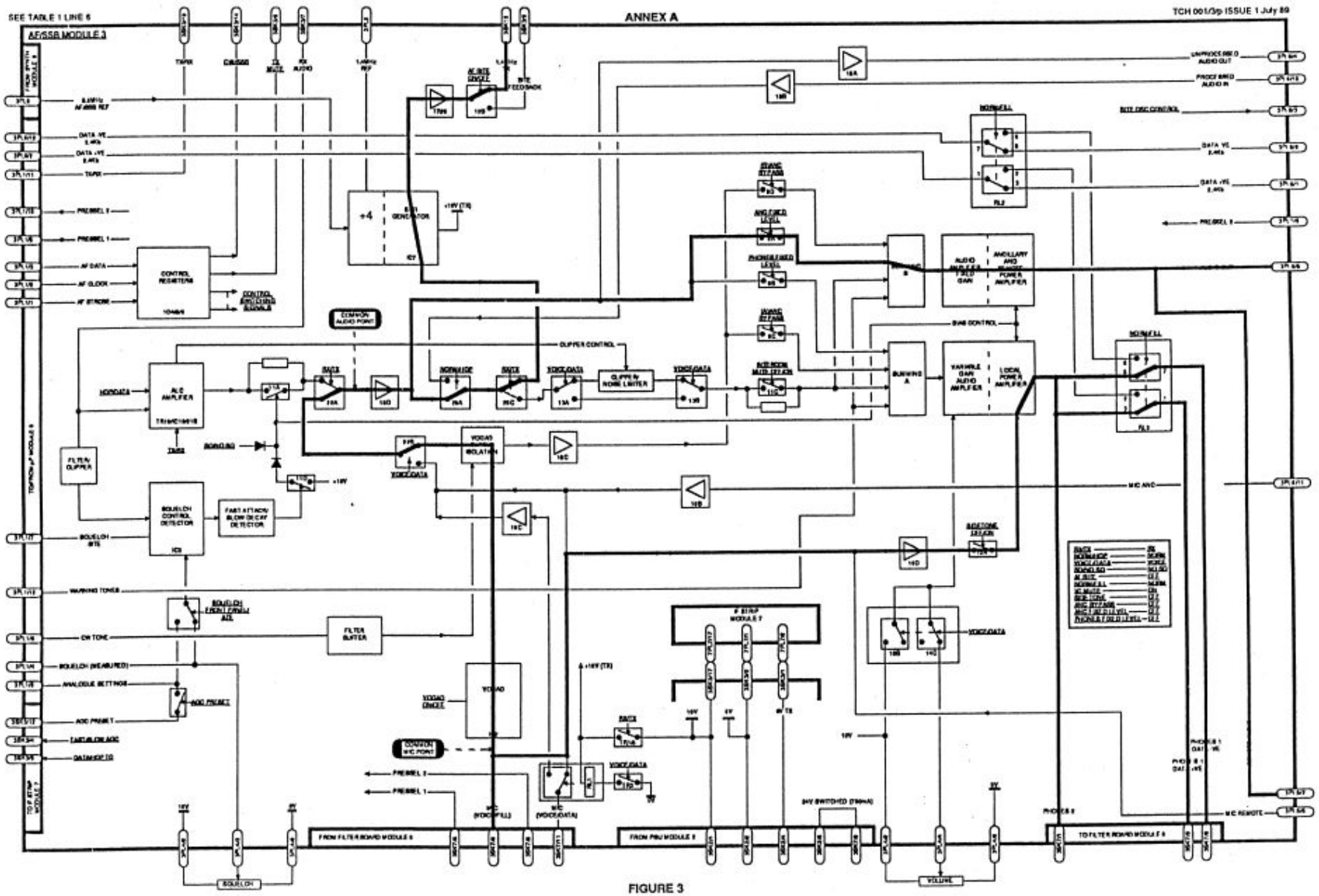


FIGURE 3

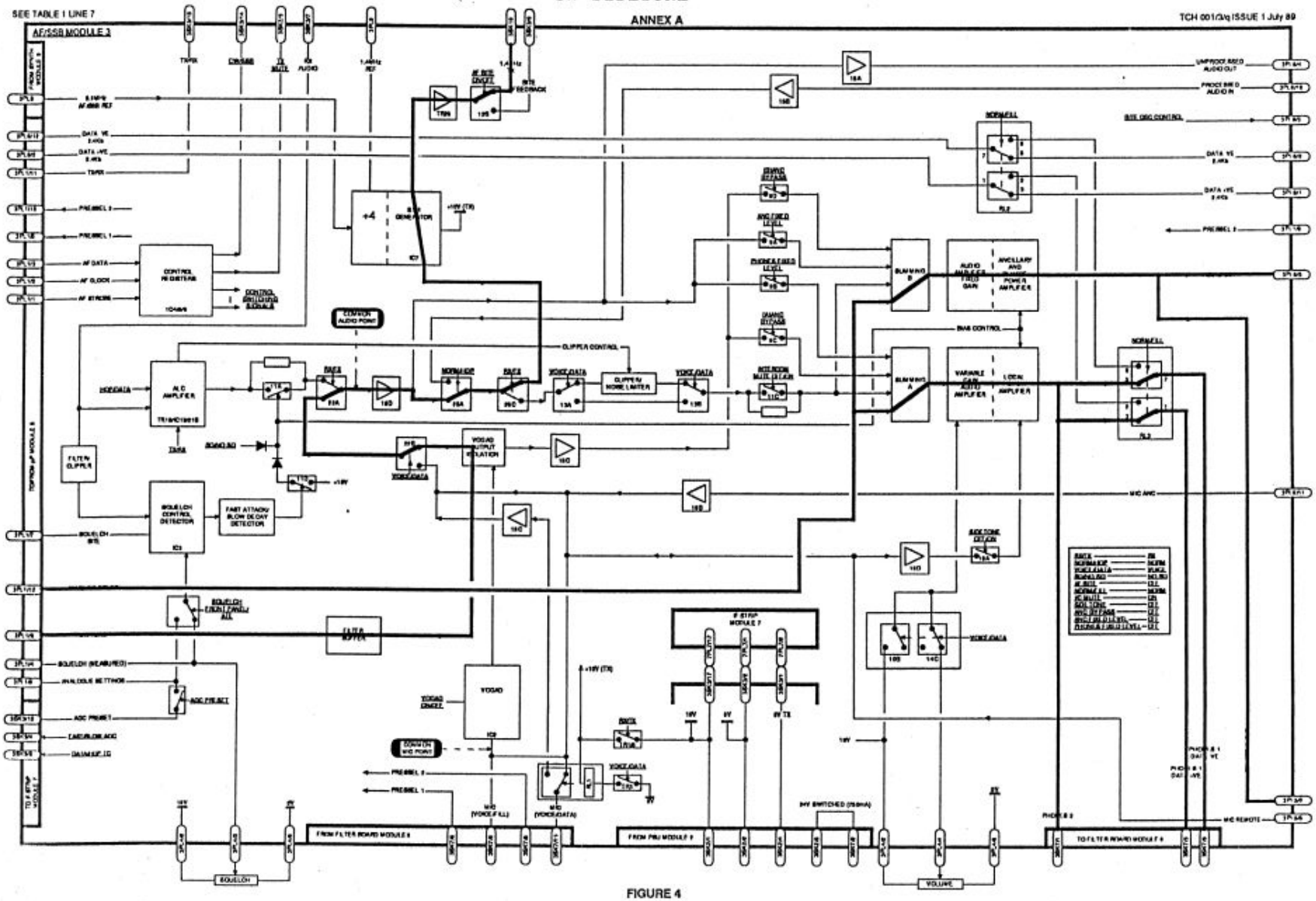

SEE TABLE 1 LINE 7
AF/SSB MODULE 3
CONTROL REGISTERS
AF DATA
AF CLOCK
AF STROBE
PRESET 2
PRESET 1
+4
CLOCK GENERATOR
CONTROL AUDIO POINT
CLIPPER CONTROL
MIC DATA
ALC AMPLIFIER
FILTER CLIPPER
SQUELCH CONTROL DETECTOR
FAST ATTACK SLOW DECAY DETECTOR
SQUELCH
FILTER BUFFER
VOGAD
VOGAD OUTPUT ISOLATION
VOGAD CIRCUIT
CONTROL MIC POINT
VOICE/DATA
CLIPPER NOISE LIMITER
SUMMING B
SUMMING A
AUDIO AMPLIFIER FIXED GAIN
AUXILLARY AND POWER AMPLIFIER
VARIABLE GAIN AUDIO AMPLIFIER
LOCAL AMPLIFIER
BIAS CONTROL
MIC AMC
VOLUME
MIC REMOTE
UNPROCESSED AUDIO OUT
PROCESSED AUDIO IN
DATA VE
DATA +VE
PRESET 2
PRESET 1
FROM FILTER BOARD MODULE 4
FROM PRU MODULE 5
TO FILTER BOARD MODULE 4

FIGURE 4

REMOTE PRESSLE SIDETONE

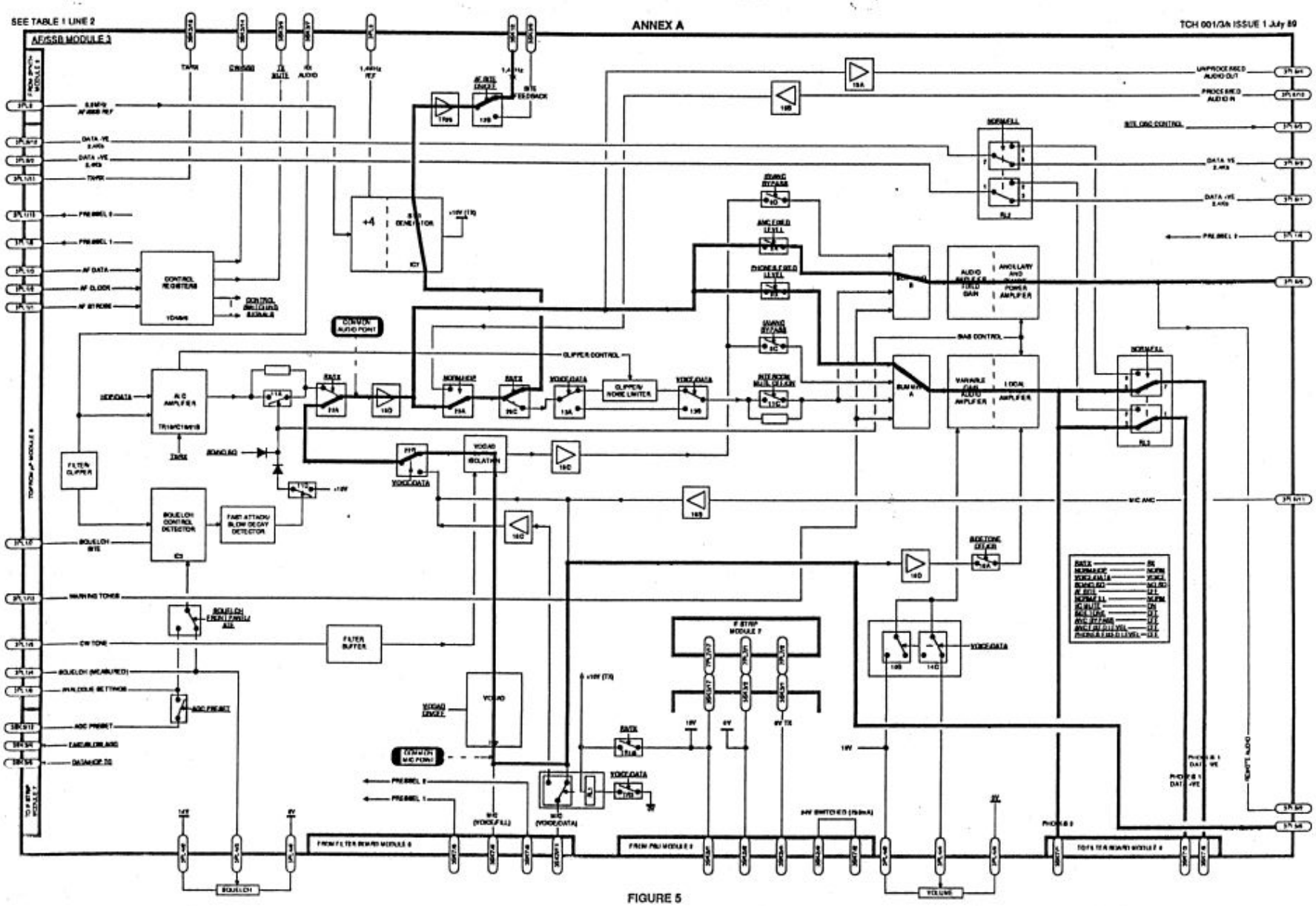


FIGURE 5

PRESSLE 1 & 2 INITIATED INTERCOM

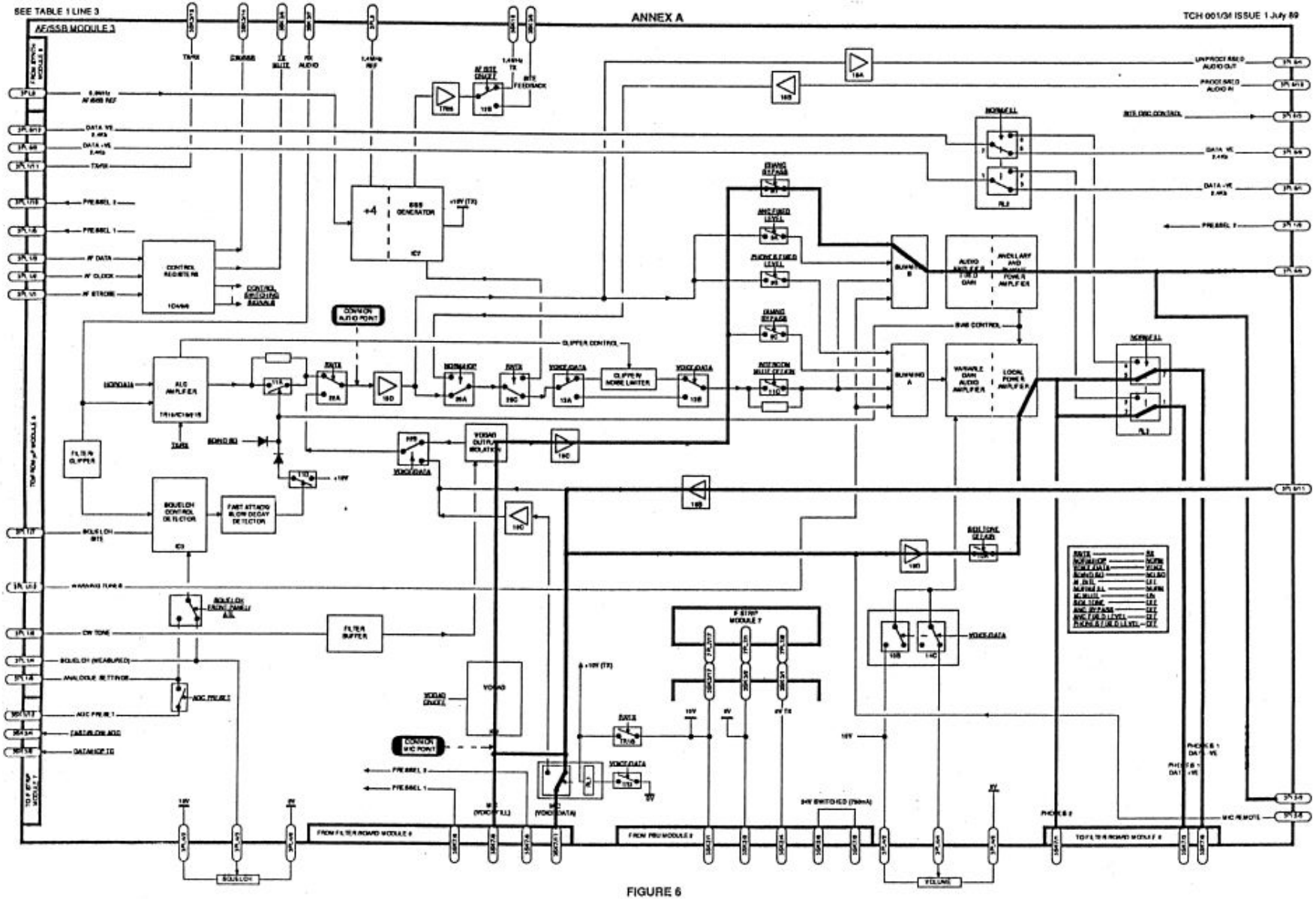


FIGURE 6

REMOTE INITIATED INTERCOM

ANNEX A

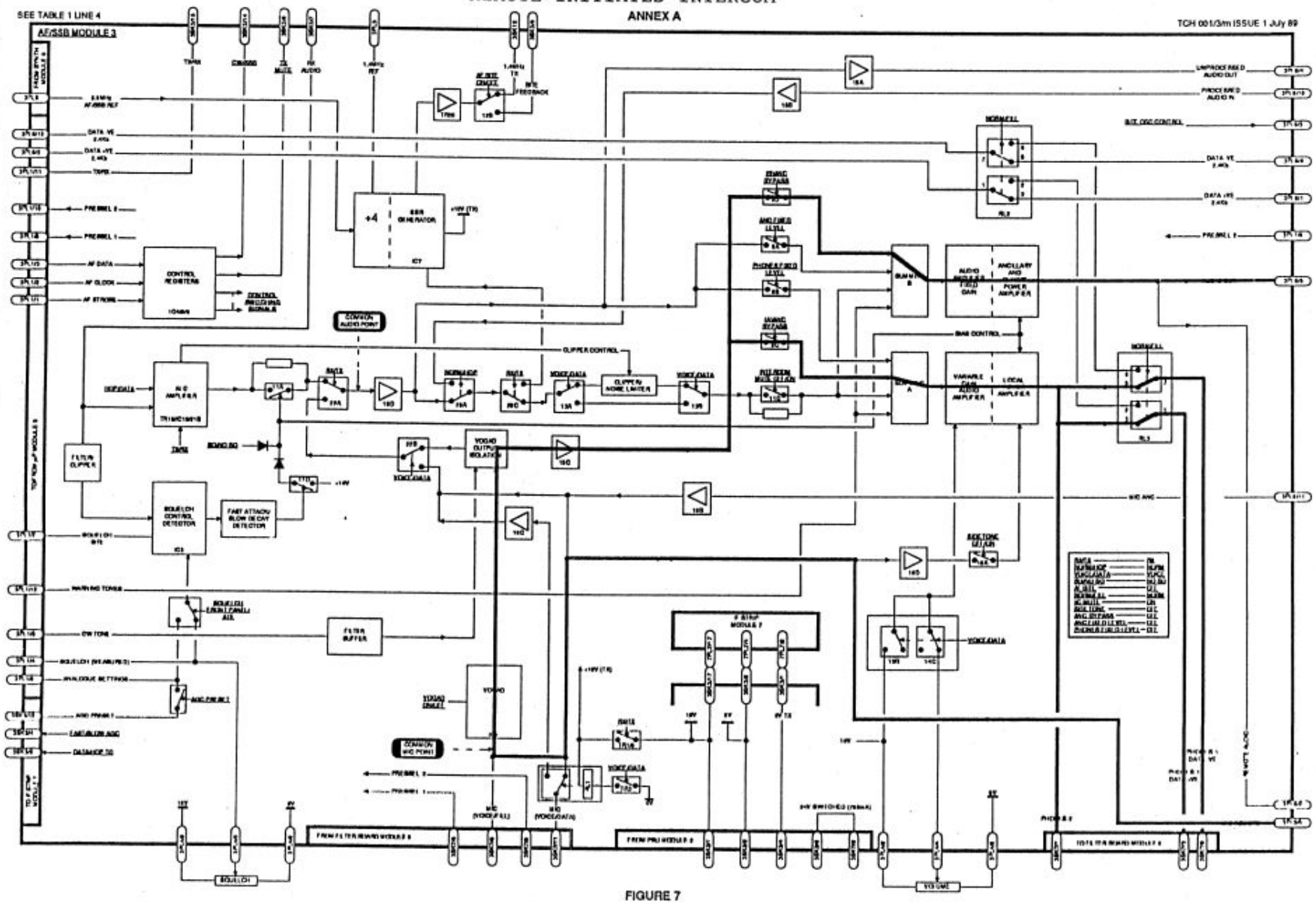


FIGURE 7

ANNEX B

CONTROL CABLE

PIN	SIGNAL NAME	PIN	SIGNAL NAME
A	READY	L	SYSTEM ON
B	FAULT	M	2FS
C	28V	N	28V
D	EXT UNIT PRESENT	P	PA CONTROL
E	EARTH	R	EARTH
F	Tx/Rx	S	ATU PROT (1)
G	RESET	T	—
H	RELAY CONTROL	U	ALC
J	PA PRESENT/ ATU PROT(2)	V	—
K	CSF PRESENT		

TABLE 1.

ANNEX C

OPEN COLLECTOR SIGNALLING

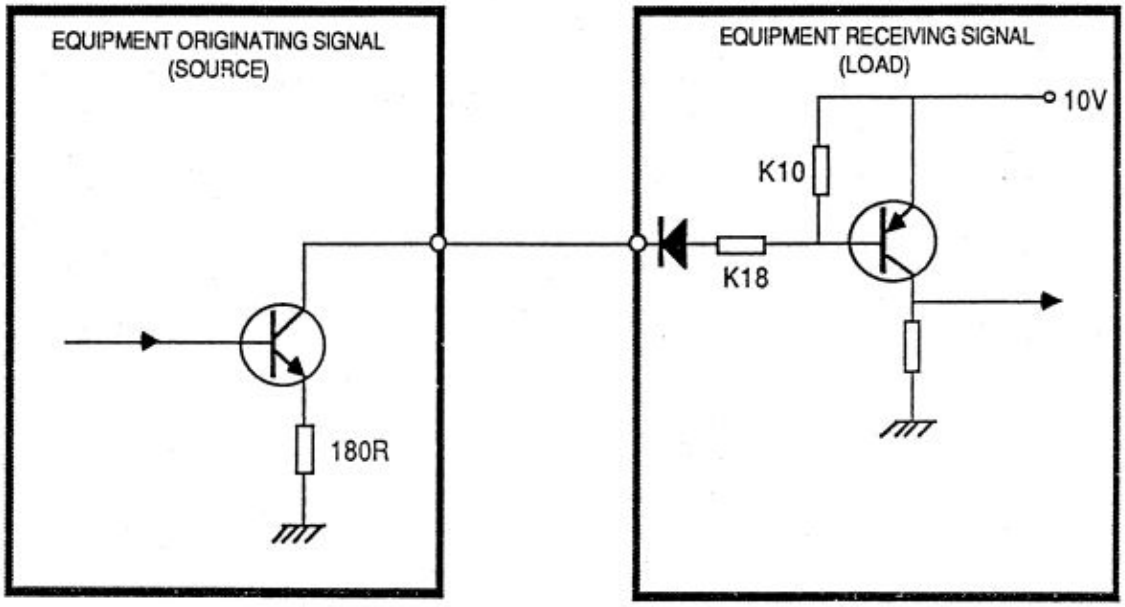


FIGURE 1.

1. The term 'Open Collector' refers to the configuration of the circuitry which makes the signal line the connection from the source transistor to its collector load. Figure 1 illustrates the situation, with the source transistor situated in the controlling, or 'signal output', equipment and its collector load in the controlled, or 'signal input', equipment.

2. The action is as follows. When the source transistor is cut off, no current flows and the signal line will be at the 10V potential of the load supply rail. If the transistor is turned on it will conduct, bringing the potential of the signal line close to 0V. The transistor in the load circuit will also be turned on, by the voltage drop across the 10Kohm resistor, and its collector will rise to 10V, an inversion of the input logic level.

3. It can be seen from the above that testing of a source circuit can only be accomplished with a suitable load connected.